UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte GEOFFREY S. STRONGIN AND DALE E. GULICK

Appeal No. 2006-2129
Application No. 09/853,335
Technology Center 2100

Decided: March 14, 2007

Before JOSEPH F. RUGGIERO, LANCE LEONARD BARRY, and HOWARD B. BLANKENSHIP, *Administrative Patent Judges*.

BARRY, *Administrative Patent Judge*.

DECISION ON APPEAL

A patent examiner rejected claims 1-13 and 15-57. The appellants appeal therefrom under 35 U.S.C. § 134(a). We affirm.

I. BACKGROUND

The invention at issue on appeal concerns sharing asserts. Many personal computers ("PCs") use an x86 operating system to implement an x86 operating

environment. (Appeal. Br. at 3.) From a hardware point of view, complain the appellants, an x86 operating environment offers little protection of user privacy, security for corporate secrets and assets, or protection of the ownership rights of content providers. Privacy, security, and ownership (collectively "PSO") have become critical in an age of Internet-connected computers. They add that the design of the original PCs failed to anticipate PSO needs. (Spec. at 4.)

From a software point of view, opine the appellants, the x86 operating environment is equally poor for PSO. The ease of direct access to hardware via software or simply by opening the cover of a PC allows an intruder or thief to compromise most security software and devices. The PCs ease of use only adds to the problems for PSO. (*Id.* at 5.)

In contrast, the appellants' bus interface logic stores a bit, which the appellants term the "master mode bit." (*Id.*) When the master mode bit is set, the bus interface logic exchanges data only with the master device that set the bit. (*Id.*)

A further understanding of the invention can be achieved by reading the following claim.

> 1. A bus interface logic configured with a storage location configured to store a master mode bit, wherein the bus interface logic is configured to exchange data only with a master device that caused the master mode bit to be set when the master mode bit is set.

Claims 1, 2, 4-8, 10-13,[1] 15, and 30-57 stand rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,446,149 ("Moriarty"). Claims 1-13, 15, and 30-57 stand rejected under § 102(e) as anticipated by U.S. Patent No. 6,356,983 ("Parks").[2] Claims 1, 2, 4-8, 10-13, 15, 30-31, 47, and 48 stand rejected under § 102(e) as anticipated by U.S. Patent No. 6,636,921 ("Scholhamer").[3]

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[1] Although the three anticipation rejections purport to include claim 14, (Examiner's Answer at 4, 6, 10, 11, 12, 14), the claim has been canceled.

[2] Although the statement of the rejection names "Scholhamer," (*id.* at 12), the explanation thereof cites to elements of Parks, (*id.* at ll. 10-12), evidencing that the rejection is actually over the latter reference.

[3] Although the statement of the rejection names "Parks", (*id.* at 10), the explanation thereof references elements of Scholhamer, (*id.* at ll. 10-12), evidencing that the rejection is actually over the latter reference.

Claims 16-29 stand rejected under 35 U.S.C. § 103(a) as obvious over Moriarty and U.S. Patent No. 6,651,168 ("Kao").

II. OPINION

Our opinion addresses the rejections in the following order:

- rejections relying on Moriarty
- rejection relying on Parks
- rejection relying on Scholhamer.

A. REJECTIONS RELYING ON MORIARTY

"When multiple claims subject to the same ground of rejection are argued as a group by appellant, the Board may select a single claim from the group of claims that are argued together to decide the appeal with respect to the group of claims as to the ground of rejection on the basis of the selected claim alone. Notwithstanding any other provision of this paragraph, the failure of appellant to separately argue claims which appellant has grouped together shall constitute a waiver of any

argument that the Board must consider the patentability of any grouped claim separately." 37 C.F.R. § 41.37(c)(1)(vii) (2005).[4]

Here, the appellants argue claims 1, 2, 4-8, 10-13, 15, and 30-57, which are subject to the same ground of rejection, as a group. (Appeal Br. at 7.) We select claim 1 as the sole claim on which to decide the appeal of the group.

"With this representation in mind, rather than reiterate the positions of the examiner or the appellants *in toto*, we focus on the point of contention therebetween." *Ex parte Morris*, No. 2005-0439, 2005 WL 4779247, at *3 (B.P.A.I. 2005). The examiner makes the following findings.

> As per claim 1, Moriarty discloses a bus interface logic (bridge) configured with a storage location (address space/semaphore memory cell; abstract) configured to store a master mode bit (semaphore memory cell; abstract; col. 2, lines 16-23), wherein the bus interface logic is configured to exchange data only with a master device that caused the master mode bit to be set when the master mode bit is set

[4] We cite to the version of the Code of Federal Regulations in effect at the time of the Appeal Brief.

> (col. 2, lines 16-35; col. 5, lines 4-13; col. 6, lines 1-15; col. 8, lines 18-67; col. 11, lines 35-46).

(Examiner's Answer at 4.) The appellants make the following allegation.

> Appellant [sic] has clearly defined the term, "master mode bit," as a bit that indicates that one or more bus interface logics or other devices will be used to establish a secure transmission channel between a master mode logic and a data input device while operating outside the operating system. See, *e.g.,* Patent Application, page 93, 11. 23-24 and page 94, line 2 - page 96, line 8, as well as Figures 36 and 37.

(Appeal Br. at 7.) Based on this allegation they argue, "Moriarty fails to describe a master mode bit." (*Id.*)

"In addressing the point of contention, the Board conducts a two-step analysis. First, we construe the representative claim at issue to determine its scope. Second, we determine whether the construed claim is anticipated." *Ex parte Pittaro*, No. 2005- 2057, 2006 WL 1665401, at *2 (B.P.A.I. 2006).

1. Claim Construction

"Analysis begins with a key legal question — what is the invention claimed?" *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1567, 1 USPQ2d 1593, 1597 (Fed. Cir. 1987). In answering the question, "the PTO gives claims their 'broadest reasonable interpretation.'" *In re Bigio*, 381 F.3d 1320, 1324, 72 USPQ2d 1209, 1211 (Fed. Cir. 2004) (quoting *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1668 (Fed. Cir. 2000)). Although "[c]laims must be read in view of the specification, of which they are a part," *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979, 34 USPQ2d 1321, 1329 (Fed. Cir. 1995) (en banc), "limitations are not to be read into the claims from the specification." *In re Van Geuns*, 988 F.2d 1181, 1184, 26 USPQ2d 1057, 1059 (Fed. Cir. 1993) (citing *In re Zletz*, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989)).

Here, claim 1 recites in pertinent part the following limitations: "a master mode bit, wherein the bus interface logic is configured to exchange data only with a master device that caused the master mode bit to be set when the master mode bit is set." The aforementioned language on which the appellants rely, viz., establishing a

secure transmission channel between a master mode logic and a data input device while operating outside the operating system, is absent from the claim. Turning to the specification, moreover, we agree with the examiner's finding, (Examiner's Answer at 22), that the disclosure of "[t]he master mode logic and the data input device exchang[ing] data outside the operating system of the computer system through the bus interface logics or other devices that include the master mode register, in block 4815," (Spec. at 95), refers to operations of the unclaimed master mode logic and data input device. Giving the representative claim the broadest, reasonable construction, therefore, the limitations require that when at least one bit is set, bus interfacing logic exchanges data only with the master device that set the bit or bits.

2. Anticipation Determination

"Having construed the claim limitations at issue, we now compare the claims to the prior art to determine if the prior art anticipates those claims." *In re Cruciferous Sprout Litig.*, 301 F.3d 1343, 1349, 64 USPQ2d 1202, 1206 (Fed. Cir. 2002). "[A]nticipation is a question of fact." *Hyatt*, 211 F.3d at 1371, 54 USPQ2d

at 1667 (citing *Bischoff v. Wethered*, 76 U.S. (9 Wall.) 812, 814-15 (1869); *In re Schreiber*, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997)). "A reference anticipates a claim if it discloses the claimed invention 'such that a skilled artisan could take its teachings in combination with his own knowledge of the particular art and be in possession of the invention.'" *In re Graves*, 69 F.3d 1147, 1152, 36 USPQ2d 1697, 1701 (Fed. Cir. 1995) (quoting *In re LeGrice*, 301 F.2d 929, 936, 133 USPQ 365, 372 (CCPA 1962)).

Here, we find that Moriarty "provides a synchronization memory address space and synchronization memory protocol for communication between multiple busmasters in a computer system." (Col. 2, ll. 14-16). The "memory address space is preferably located in a memory controller embedded in a peripheral device such as a bridge that provides central, high speed access by a busmaster to the memory controller. . . ." (*Id.* at ll. 17-20). Because "[a] host/PCI bridge serves as a connection between a host bus and a PCI bus," (col. 3, ll. 60-61), we also find that the bridge constitutes bus interfacing logic.

"The [aforementioned] address space includes a set of semaphore memory cells mapped to shared critical resources in the computer system. Each region of the self-modifying synchronization address space corresponding to a particular shared critical resource serves as a synchronization memory channel." (Col. 2, ll. 21-26.) Each "semaphore memory cell 60 is preferably implemented as a semaphore memory bit 84." (Col. 8, ll. 19-21.) The semaphore memory bit "allows for exclusive access by a busmaster to a shared critical resource by switching itself from an idle state to a busy state responsive to a first read operation by a busmaster." (Col. 2, ll. 27-30.)

We agree with the examiner's finding that when the semaphore memory bit is set in the busy state, the host/PCI bridge exchanges data only with the busmaster that set the bit. To wit, "[i]n the busy state of the semaphore memory cell, a busy state is communicated to other busmasters which attempt to read the semaphore memory cell." (*Id.* at ll. 30-33.) In contrast, "[n]umerous read operations may be performed," (col. 9, ll. 54-55), by the busmaster that performed the first read operation.

Because the host/PCI bridge exchanges data only with the busmaster that set the semaphore memory bit to the busy state, we find that a skilled artisan could take Moriarty's teachings in combination with his own knowledge of the particular art and be in possession of the invention. Therefore, we affirm the rejection of claim 1 and of claims 2, 4-8, 10-13, 15, and 30-57, which fall therewith.

Rather than arguing the rejection of claims 16-29 separately, the appellants rely on the aforementioned argument. (Appeal Br. at 9-10.) Unpersuaded by these arguments, we also affirm the rejections of these claims.

B. REJECTION RELYING ON PARKS

The appellants argue claims 1-13, 15, and 30-57, which are subject to the same ground of rejection, as a group. (Appeal Br. at 8-9.) We select claim 1 as the sole claim on which to decide the appeal of the group.

The examiner makes the following findings.

> As per claims 1 and 3, [Parks] discloses a bus interface logic (çol. 7, lines 3-10) configured with a storage location (303) configured to store a master mode bit, wherein the bus interface logic is configured to exchange data only with a master device that caused the master mode bit to be set when the master mode bit is set (col. 9, lines 19-33; col. 12, lines 50-53; see also Table 5).

(Examiner's Answer at 12.) The appellants make the following argument.

> Park [sic] does not describe or suggest a master mode bit, *i.e.* a bit that indicates that one or more bus interface logics or other devices will be used to establish a secure transmission channel between a master mode logic and a data input device while operating outside the operating system, as defined in the Patent Application.

(Appeal Br. at 8.)

1. Claim Construction

As mentioned regarding the rejections relying on Moriarty, claim 1 requires that when at least one bit is set, bus interfacing logic exchanges data only with the master device that set the bit or bits. The claim, however, is not restricted to a single bit.

2. Anticipation Determination

We find that Parks discloses "[a] cache coherency directory for a shared memory multiprocessor computer system." (Abs. at ll. 1-2.) The "[m]ultiprocessor computer system 100 incorporates N processor boards 101," (col. 5, ll. 36-38), which "are bidirectionally coupled to shared memory 103. . . ." (*Id.*) "Shared memory 103 is configured as a plurality M of memory banks 105." (*Id.* at ll. 52-53.)

A "[c]ache coherency directory 303 includes a multi-bit entry for each memory line (i.e., cache line) in the shared memory address space of the particular memory bank data portion 320. The entry contains a value indicating the current

state of the corresponding memory line." (Col. 7, ll. 5-9.) "FIG. 4 shows an exemplary cache coherency directory entry 400." (Col. 8, ll. 37-38.) "[B]its <21:25> hold a current directory processor node ID (DID) value." (Col. 9, ll. 10-11.) "In the exclusive state the DID field holds a node ID value identifying the processor node 101 that holds exclusive access." (*Id.* at ll. 19-21.) "While a node has exclusive access to a cache line, any operation by the owning node (i.e., DID) is permitted." (Col. 12, ll. 51-53.)

Because bits 21:25 hold a value identifying the processor node 101 that holds exclusive access, we find that a skilled artisan could take Parks teachings in combination with his own knowledge of the particular art and be in possession of the invention. Therefore, we affirm the rejection of claim 1 and of claims 2-13, 15, and 30-57, which fall therewith.

C. REJECTION RELYING ON SCHOLHAMER

"The PTO Rules of Practice require the examiner to cite only what he considers the 'best references.'" *E.I. duPont de Nemours & Co. v. Berkley & Co.*, 620 F.2d 1247, 1266, 205 USPQ 1, 16 (8th Cir. 1980). "The examiner is not called upon to cite all references that may be available, but only the 'best.'" MPEP § 904.03 (8th ed. rev. 4 Oct. 2005) (quoting 37 C.F.R. § 1.104(c)). *See also* MPEP § 706.02 ("Prior art rejections should ordinarily be confined strictly to the best available art.") "Multiplying references, any one of which is as good as, but no better than, the others, adds to the burden and cost of prosecution and should therefore be avoided." *Id.* at § 904.03.

Here, the fact that Scholhamer has been relied on to reject only a subset of those claims already rejected as anticipated by Moriarty or Parks evidences that the former reference is no better than the latter two references. The examiner should avoid such multiplication of references.

The examiner makes the following findings.

> As per claims 1, 30 and 47, [Scholhamer] discloses system and method comprising: a bus interface logic (repeater and repeater control & status registers; fig. 3, 4 or 10) configured with a storage location (status registers or ID registers) configured to store a master mode bit (initiator ID; col. 8, lines 26-28 and 40-67), wherein the bus interface logic is configured to exchange data only with a master device that caused the master mode bit to be set when the master mode bit is set (col. 8, lines 26-28 and 40-67).

(Examiner's Answer at 10.) The appellants argue, "Scholhamer does not describe or suggest a master mode bit . . . ." (Appeal. Br. at 8.)

"In addressing the point of contention, the Board conducts a two-step analysis. First, we construe the independent claims at issue to determine their scope. Second, we determine whether the construed claims are anticipated." *Ex parte Wang*, No. 2003-0513, 2004 WL 4978835, at *2 (B.P.A.I. 2004).

1. Claim Construction

Independent claim 1 recites in pertinent part the following limitations: "a storage location configured to store a master mode bit, wherein the bus interface

logic is configured to exchange data only with a master device that caused the master mode bit to be set when the master mode bit is set." Independent claims 7, 30, and 47 recite similar limitations. Giving the independent claims the broadest, reasonable construction, the limitations require a storage location for at least one bit such that when the bit is set, bus interfacing logic exchanges data only with the master device that set the bit or bits.

2. Anticipation Determination

"[A]bsence from the reference of any claimed element negates anticipation." *Kloster Speedsteel AB v. Crucible, Inc.,* 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986). Here, Scholhamer "relates to a repeater circuit for providing effective point-to-point coupling between terminated Small Computer System Interface (SCSI) bus segments." (Abs. at ll. 1-3). "The repeater circuit has an enable input and can perform SCSI address translation to map SCSI addresses from a narrow SCSI bus to high SCSI addresses on a wide SCSI bus." (*Id.* at ll. 3-6.) The first set of lines of the reference cited by the examiner disclose that "during a SCSI address phase, each of the data signals, or bits, on SCSI bus 200 correspond

to a SCSI ID with initiator 220 occupying one SCSI ID on SCSI bus 200." (Col. 8, ll. 26-28).

"The address phases include ARBITRATION, SELECTION and RESELECTION SCSI bus phases." (*Id.* at ll. 28-30.) The second set of lines of Scholhamer cited by the examiner explain that "[u]pon completing the ARBITRATION phase, the winning SCSI target then sets the data bus of SCSI bus 204 or 202 to a value that is the logical OR of the target's SCSI ID and the initiator's SCSIID." (*Id.* at ll. 54-57.) We are unpersuaded, however, that the data bus constitutes a storage location. Although the reference's "repeater circuit 100 is connected to repeater control and status registers (RCSR) 511 through an APB bus 551," (col. 6, ll. 34-35), we are likewise unpersuaded that the registers store the value of the data bits on SCSI bus 200 therein.

The absence require a storage location for at least one bit such that when the bit is set, bus interfacing logic exchanges data only with the master device that set the bit or bits negates anticipation. Therefore, we reverse the rejection of

claims 1, 7, 30, and 47, and of claims 2, 4-6, 8, 10-13, 15, 31, and 48, which depend therefrom.

III. CONCLUSION

In summary, the rejection of claims 1, 2, 4-8, 10-13, 15, and 30-57 as anticipated by Moriarty and the rejection of claims 16-29 as obvious over Moriarty and Kao are affirmed. The rejection of claims 1-13, 15, and 30-57 as anticipated by Parks is also affirmed. In contrast, the rejection of claims 1, 2, 4-8, 10-13, 15, 30-31, 47, and 48 as anticipated by Scholhamer is reversed.

"Any arguments or authorities not included in the brief or a reply brief filed pursuant to [37 C.F.R.] § 41.41 will be refused consideration by the Board, unless good cause is shown." 37 C.F.R. § 41.37(c)(1)(vii). Accordingly, our affirmance is based only on the arguments made in the brief. Any arguments or authorities omitted therefrom are neither before us nor at issue but are considered waived. *Cf. In re Watts*, 354 F.3d 1362, 1367, 69 USPQ2d 1453, 1457 (Fed. Cir. 2004) ("[I]t is important that the applicant challenging a decision not be permitted to raise

arguments on appeal that were not presented to the Board.") No time for taking any action connected with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

JOSEPH F. RUGGIERO
Administrative Patent Judge

LANCE LEONARD BARRY
Administrative Patent Judge

HOWARD B. BLANKENSHIP
Administrative Patent Judge

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